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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/900,407	07/06/2001	Rolf Fritz	DE20000059.USI	5093
7590 12/23/2004			EXAMINER	
Lynn L. Augspurger IBM Corporation Intellectual Property Law 2455 South Road, P386 Poughkeepsie,, NY 12601			MAURO JR, THOMAS J	
			ART UNIT	PAPER NUMBER
			2143	
DATE MAILED: 12/23/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/900,407	Applicant(s) FRITZ ET AL.	
	Examiner Thomas J. Mauro Jr.	Art Unit 2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 July 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 and 18-27 is/are rejected.
- 7) ☒ Claim(s) 17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 July 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>20011015</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-27 are pending and are presented for examination. A formal action on the merits of claims 1-27 follows.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file. Priority date, therefore, for this application is 08/03/2000.

Drawings

The drawings are objected to because they fail to show the necessary textual labels of the various features in Figures 1, 3 and 4. Each element in Figures 1, 3 and 4 must be labeled as described in the specification. A descriptive textual label for each numbered element in the figures would be necessary for one to fully understand the figures without substantial analysis of the detailed specification. Any structural detail that is of sufficient important to be described should be shown and properly labeled in the drawings. See 37 CFR 1.84(n) and (o). A proposed drawing correction or corrected drawings are required in replay to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-3, 11-13, 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalkunte (U.S. 6,138,189) in view of Sartain et al. (U.S. 6,678,243).

Regarding claim 1, Kalkunte teaches a method comprising the steps of:

starting to write data into said buffer [Kalkunte -- **Figure 1 and Col. 3 line 67 – Col. 4 lines 1-8 – Data is written into the buffer from the CPU**];

waiting for a predetermined delay time [Kalkunte -- **Figures 1 and 3, Col. 4 lines 40-47 and Col. 5 lines 63-67 – Col. 6 lines 1-8 – Before transmission occurs, transmit start point delay value is predetermined if it should be set to minimum or adjusted to difference in arrival and removal, i.e. write/read, rates. Thus, for example, delay is set to $X_m + \Delta m$**];

starting to read data from said buffer after said delay time has passed [Kalkunte -- **Figure 1, Col. 2 lines 22-27 and Col. 4 line 7-8 – Data is read from the buffer after the delay time has passed**];

determining the length of a time gap between the completion of writing data into said buffer and completion of reading data from said buffer [Kalkunte -- **Col. 6 lines 2-3 – Δt is calculated which is the difference in time, i.e. gap, between packet filling, i.e. writing data, and packet removal, i.e. reading data, from the buffer**]; and

decreasing the length of said delay by a first value if the gap is larger [**Kalkunte -- Col. 4 lines 29-45, Col. 5 lines 47-62 and Col. 6 lines 17-22** – For each packet that enters the buffer, a determination is made as to whether the delay currently in use is adequate. For example, if delay time is currently $X_m + \Delta m$ and the time for removal is greater than or equal time to fill, then delay is decreased to X_m].

While Kalkunte clearly teaches calculating a length of time gap, i.e. Δt , he fails to teach comparing it to a tolerance, i.e. threshold value.

Sartain, however, discloses a system for preventing buffer overflow and underrun conditions by adjusting the reading rate, i.e. delay, based upon whether or not it meets a definable low or high threshold [**Sartain -- Col. 3 lines 22-31, Col. 5 lines 48-55 and Col. 6 lines 17-18 and lines 29-40**].

Both Kalkunte and Sartain solve problems in the same field of endeavor, namely preventing underrun buffer situations by adjusting delay periods.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the tolerance, i.e. threshold, values for comparison, as taught by Sartain in order to expand the latency adjusting mechanism of Kalkunte, in order to provide a more adaptive buffering system which allows for dynamic compensation of differing data rates thereby providing more granularity in altering delays [**Sartain -- Col. 1 lines 63-64**].

Regarding claim 2, Kalkunte-Sartain teach the invention substantially as claimed, as aforementioned in claim 1 above, including increasing the length of said delay if the length of said time gap is smaller [**Kalkunte -- Col. 4 lines 29-45 and Col. 5 lines 63-67 - Col. 6 lines 1-**

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22 – For each packet that enters the buffer, a determination is made as to whether the delay currently in use is adequate. For example, if delay time is currently X_m and the time for removal is less than the time to fill, then delay is increased to $X_m + \Delta m$, where Δm is the differential buffer capacity time] than a specified tolerance value [Sartain -- Col. 3 lines 22-31, Col. 5 lines 48-55 and Col. 6 lines 17-18 and lines 29-40 – Low and high threshold, i.e. tolerance, values trigger delay adjustments].

Regarding claim 3, Kalkunte-Sartain teach the invention substantially as claimed, as aforementioned in claim 2 above, including storing the length of said delay [**Kalkunte -- Figure 1, Col. 6 lines 39-43 and lines 48-51 – Adaptive start point value, i.e. delay, (XMTSP) is output from the setting means within the FIFO control, thereby indicating the value was stored previously so that it could be output].**

Regarding claim 11, Kalkunte teaches a device comprising:

a memory unit for storing a predetermined delay time [**Kalkunte -- Figure 1, Col. 6 lines 39-43 and lines 48-51 – Adaptive start point value, i.e. delay, (XMTSP) is output from the setting means within the FIFO control, thereby indicating the value was stored, i.e. in memory, register, etc., previously so that it could be output]; and**

a counter for measuring a delay time [**Kalkunte -- Col. 6 lines 32-38 – Counter measures time necessary for delays];**

The remaining limitations of claim 11 are similar to the limitations claimed in the method of claim 1. Therefore, claim 11 is rejected under the same rationale.

Regarding claims 12 and 13, these are device claims corresponding to the method claimed in claims 2 and 3 above. They have similar limitations; therefore, claims 12 and 13 are rejected under the same rationale.

Regarding claim 18, Kalkunte teaches a computer program with software code for performing the invention [**Kalkunte -- Col. 3 lines 47-67 – Col. 4 lines 1-14 – Instructions written into the various units, i.e. FIFO control, buffer management unit, provide control for invention**]. The remaining limitations of claim 18 are similar to the limitations claimed in the method of claim 1. Therefore, claim 18 is rejected under the same rationale.

Regarding claims 19 and 20, these are computer program claims corresponding to the method claimed in claims 2 and 3 above. They have similar limitations; therefore, claims 19 and 20 are rejected under the same rationale.

5. Claims 4-6, 14 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalkunte (U.S. 6,138,189) and Sartain et al. (U.S. 6,678,243), as applied to claims 3, 13 and 20 above respectively, in view of Mangin et al. (U.S. 5,982,778).

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Regarding claim 4, Kalkunte-Sartain teach the invention substantially as claimed, as aforementioned in claim 3 above, including wherein data packets of varying size are written into and read from said buffer [**Kalkunte -- Col. 2 lines 22-27, Col. 6 lines 32-38 and lines 56-61 -- Data packets having varying lengths are written into and read out of the buffer**], but fails to explicitly teach, although suggests, that data packets are classified according to their size and a delay is selected based upon the packet size.

Mangin, however, discloses a system for regulating the rate of data transmission on a network by adjusting the delay time of packets exiting a buffer based upon the size of the packet as it is classified [**Mangin -- Col. 2 lines 27-29, Col. 4 lines 26-29, Col. 6 lines 5-14 and Col. 7 lines 1-14**].

Both Kalkunte-Sartain and Mangin are concerned with the same field of endeavor, namely, adjusting the delay time of packets leaving a buffer.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the classifying of packets based upon length to determine the delay, as taught by Mangin into the invention of Kalkunte-Sartain, in order to maintain an overall constant output transmission rate [**Mangin -- Col. 6 lines 13-14**].

Regarding claim 5, Kalkunte-Sartain-Mangin teach the invention substantially as claimed, as aforementioned in claim 4 above, including wherein writing said data into said buffer is interrupted by a specified number of breaks of a known maximum length and wherein said tolerance value is larger than the sum of the lengths of the specified number of breaks [**Kalkunte -- Col. 5 lines 40-45 and Col. 6 lines 3-11 -- Burst transmission, i.e. transmission of spurts**]

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and idle times, is factored in along with bus latency times of PCI bus and other characteristics. The coefficient 'a' is factored into a tolerance value to ensure that the tolerance is larger than the breaks, i.e. latencies and spurt delays].

Regarding claim 6, Kalkunte-Sartain-Mangin teach the invention substantially as claimed, as aforementioned in claim 5 above, including wherein said determining the length of said time gap [**Kalkunte -- Col. 6 lines 2-3 – Δt is calculated which is the difference in time, i.e. gap, between packet filling, i.e. writing data, and packet removal, i.e. reading data, from the buffer**] includes correcting the length of said gap by the total length of the breaks that occurred during writing the data into said buffer [**Kalkunte -- Col. 5 lines 40-45 and Col. 6 lines 3-11 – Length of said time gap is corrected by correcting one of its components, namely t_p or packet fill time, which involves factoring in the breaks and latency, namely 'a', when data is being written into the buffer**].

Regarding claim 14, this is a device claim corresponding to the method claimed in claim 4 above. It has similar limitations; therefore, claim 14 is rejected under the same rationale.

Regarding claims 21-23, these are computer program claims corresponding to the method claimed in claims 4-6 above. They have similar limitations; therefore, claims 21-23 are rejected under the same rationale.

6. Claims 7-10, 15-16 and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalkunte (U.S. 6,138,189), Sartain et al. (U.S. 6,678,243) and Mangin et al. (U.S. 5,982,778), as applied to claims 6, 14 and 23 above respectively, in view of Sasaki (U.S. 6,556,568).

Regarding claim 7, Kalkunte-Sartain-Mangin teach the invention substantially as claimed, as aforementioned in claim 6 above, but fails to explicitly teach writing dummy data into said buffer during idle time.

Sasaki, however, discloses a buffering system which minimizes delay and prevents underrun which includes writing dummy data into a time slot [**Sasaki -- Col. 7 lines 44-56**].

Sasaki, along with Kalkunte-Sartain-Mangin are all concerned with reducing delays when buffering data.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the writing of dummy data into a buffer, as taught by Sasaki into the invention of Kalkunte-Sartain-Mangin, in order to prevent situation where lack of transmission data exists thereby allowing the continuity of transmitted data to no longer be lost [**Sasaki -- Col. 7 lines 54-56**].

Regarding claim 8, Kalkunte-Sartain-Mangin-Sasaki teach the invention substantially as claimed, as aforementioned in claim 7 above, including generating a signal that occurs a specified number of cycles, i.e. time, before all data are read from said buffer [**Sartain -- Col. 3**

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lines 7-9 and Col. 4 lines 16-18 – Monitor generates a signal at a specified time when a buffer has an amount of data to be read below some low threshold, i.e. before all data is read from said buffer].

Regarding claim 9, Kalkunte-Sartain-Mangin-Sasaki teach the invention substantially as claimed, as aforementioned in claim 8 above, including wherein said specified number of cycles corresponds to the tolerance value **[Sartain -- Col. 3 lines 7-9 and Col. 4 lines 16-18 – Monitor generates a signal at a specified time which corresponds to the low threshold, i.e. tolerance].**

Regarding claim 10, Kalkunte-Sartain-Mangin-Sasaki teach the invention substantially as claimed, as aforementioned in claim 9 above, including detecting a read buffer signal, but fails to explicitly teach detecting a signal of whether the writing into said buffer is done or still going on. Sartain discloses above detecting a signal during the reading of data from a buffer **[Sartain -- Col. 3 lines 7-9 and Col. 4 lines 16-18 – Monitor generates a signal at a specified time when a buffer has an amount of data to be read below some low threshold, i.e. before all data is read from said buffer].**

Because buffers and signaling of levels of data in buffers were notoriously well-known in the art, it would have been obvious to a person of ordinary skill in the art that the same type of signal could be used to monitor the writing of data to a buffer in the same manner to detect if writing is occurring or not.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the signal for monitoring the writing of data into a buffer, as

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would have been obvious to one of ordinary skill in the art into the invention of Kalkunte-Sartain-Mangin-Sasaki, in order to provide monitoring and notification of whether data continues to be written which, depending on the reading of the data, can lead to a overrun situation.

Regarding claims 15 and 16, these are device claims corresponding to the method claimed in claims 8 and 10 above. They have similar limitations; therefore, claims 15-16 are rejected under the same rationale.

Regarding claims 24-27, these are computer program claims corresponding to the method claimed in claims 7-10 above. They have similar limitations; therefore, claims 24-27 are rejected under the same rationale.

Allowable Subject Matter

7. Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Williams et al. (U.S. 6,715,007) discloses a method of regulating a flow of data in a buffering system based upon thresholds.
- Castellano (U.S. 6,408,349) discloses an adjustable buffer to compensate for read/write drift.
- Graumann et al. (U.S. 6,665,728) discloses establishing optimal latency in streaming data applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Mauro Jr. whose telephone number is 571-272-3917. The examiner can normally be reached on M-F 8:00a.m. - 4:30p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A. Wiley can be reached on 571-272-3923. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

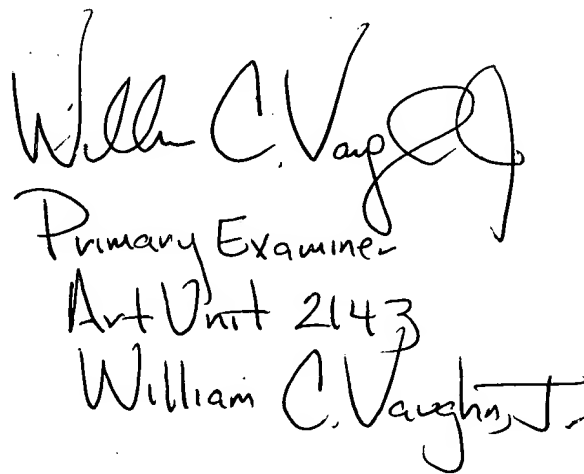
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TJM

December 8, 2004



Primary Examiner
Art Unit 2143
William C. Vaughn, Jr.